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INFO	TION	DISCLOS	URE	First Named Inventor		Jonathan S. Turner	
STAT	NT B	Y APPLIC	ANT	Group Art Unit		2662	
					Exan	niner Name	QURESHI, AFSAR M
Sheet	1	1	of	1	Attor	mey Docket No.	39209
			U.S. PAT	TENT DOCUM	ENTS	3	
EXAMINER'S INITIALS	Cite No.	1		ISSUE o		Name of Patentee or Applicant of Cited Document	
Res	AA	US - 5402415		03-28-19	95	Jonathan S. Turner	
NS	AB	US - 5229991		07-20-19	93	Jonathan S. Turner	
nel	AC	US - 5260935		11-09-19	93	Jonathan S. Turner	
res	AD	US - 5339311		08-16-19	94	Jonathan S. Turner	
Re(AE	US - 5179556		01-12-19	93	Jonathan S. Turner	
Res	AF	US - 5179551		01-12-19	93	Jonathan S. Turr	ner
Ris	AG	US - 4901309		2-13-199	90	Jonathan S. Turn	ner
rus	AH	US - 484	US - 4849968		89	Jonathan S. Turn	
Res	AI	US - 4829227		05-09-19	89	Jonathan S. Turn	
Ris	AJ	US - 473	4907	03-29-19	88	Jonathan S. Turner	
RCS	AK	US - 449	4230	01-15-19	85	Jonathan S. Turner	
RC	AL	US - 4491945		01-01-19	85	Jonathan S. Turner	
NS	AM	US - 4630260		12-16-19	86	Toy et al.	
pes	AN	US - 4893304		01-09-19	90	Giacopelli et al.	
RUS	AM	US - 5127000		06-30-19	92	Michel A. R. Henrion	
RCS	AN	US - 5173897		12-22-19	92	Schrodi et al.	
RUS	AO	US - 5253251		10-12-19	93	Toshiya Aramaki	
RS	AP	US - 584	2040	11-24-19	11-24-1998 Hughes et al.		
EXAMINER'S INITIALS	Cite No.	OTHER DOCUMENTS					
	40	O ZURIN DITTIA "Integrated Hardware/Software Design of a High Performance Network					

E	EXAMINER'S INITIALS	Cite No.	OTHER DOCUMENTS		
pcs '		AQ	ZUBIN DITTIA, "Integrated Hardware/Software Design of a High Performance Network Interface," March 2000, Doctor of Science Thesis, Sever Institute of Technology, Washington University, St. Louis, Missouri, 139 pages.		
			JONATHAN S. TURNER, "An Optimal Nonblocking Multicast Virtual Circuit Switch," June 1994, Proceedings of Infocom, 8 pages.		
	fcs	AS CHANEY ET AL., "Design of a Gigabit ATM Switch," Feb. 5, 1996, WI Washington University, St. Louis, MO, 20 pages.			
	res	AT	TURNER ET AL., "System Architecture Document for Gigabit Switching Technology," Aug. 27, 1998, Ver. 3.5, ARL-94-11, Washington University, St. Louis, MO, 110 pages.		

Not CS Infl 10-21-09